THE UNIVERSITY OF MICHIGAN

Technical Report 12

CONCOMP

November 1968

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FLEXIBLE HIGH-SPEED INTERFACE BETWEEN IBM 1800 AND DEC PDP-7 COMPUTERS

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CONCOMP: Research in Conversational Use of Computers
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ORA Project 07449

supported by:

ADVANCED RESEARCH PROJECTS AGENCY
DEPARTMENT OF DEFENSE
WASHINGTON, D.C.

CONTRACT NO. DA-49-083 - OSA-3050
ARPA ORDER NO. 716

administered through:

OFFICE OF RESEARCH ADMINISTRATION ANN ARBOR

November 1968

ABSTRACT

The principal function of the interface is to transfer blocks of data from the memory of either computer to the memory of the other. Once initialized, the interface transfers data via cycle-steal with respect to each of the two computers' memories. Either computer can detect the status of the interface at any time during a data transfer, and can halt or modify the operation as desired. When a transfer operation has been completed, the interface can signal either or both computers. Special circuitry permits resolution of conflicts resulting from simultaneous attempts by both computers to use the interface. Provision is also included for direct signaling of either computer by the other, via an "interruption."

The operation of the interface during data-transfers is completely controlled by registers internal to itself which can be loaded by either computer; and the condition of the data-handling circuits is indicated at all times by these same registers, which can also be read by either computer. This allows the interface to be commanded fully by either computer or by both. The use of addressable registers to control the interface permits considerable and unusual flexibility in its operation.

Independent counters govern a parallel-to-serial-to-parallel data path via a shift register. This allows flexible control of

data density and format. This feature permits efficient use of data storage devices (including the computers' own memories), and is especially desirable when the two computers differ in memory word size as in this case.

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I. INTRODUCTION

This is the third of three related reports describing work performed by members of the Logic of Computers Group, a research unit of the Department of Computer and Communication Sciences at The University of Michigan.

The Logic of Computers Group computer facility consists of two, small, general-purpose computers and related peripheral equipment. It is intended to provide a vehicle for heuristic investigation of problems involving large-scale simulations of generalized adaptive systems, including a large class of biologically oriented models.

The first two reports* document those portions of the system software that are largely or completely finished, and that are not likely to undergo further substantial development. They are intended to

1. serve as a progress and research reports describing the capabilities of the current software,

2. serve as a user's manuals, and

3. provide enough system information to allow later users

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* Brender, R.F., Frantz, D.R., Foy, J.L. Jr., and Schunior, T.W., Specialized System Software for Interacting DEC PDP-7 and IBM 1800, Technical Report 11, Concomp Project, University of Michigan, Ann Arbor, October 1968.

Frantz, D.R., Brender, R.F., Foy, J.L. Jr., LOCOSS: A Multiprogramming Monitor for the DEC PDP-7, Technical Report 10, Concomp Project, University of Michigan, Ann Arbor, October 1968.

to modify or maintain the system.

The LOCOSS system for the PDP-7 and the 1800 file system are basic and flexible tools. Descriptions of several other systems components are included for completeness. The hardware configuration is summarized at the end of this section.

In general, the TSX system provided by IBM is the basic software nucleus for the 1800. LOCOSS is the basic software nucleus on the PDP-7.

LOCOSS, the Logic of Computers Operating System for the PDP-Seven, was developed to provide a suitable run-time environment in which to run application programs. It provides buffered, overlapped, and essentially device-independent input/output. A keyboard Command Interpreter provides a number of real-time control services and simple debugging aids. Multiprogramming capabilities are an essential part of the system organization and allow flexible organization of application programs. LOCOSS, in our estimation, provides unusually flexible capabilities and services on a machine of this size, and requires less than 2K (decimal) of core.

The availability of bulk storage on the 1800 disk via the "minor" 1800-PDP-7 interface (in use since April 1968) made it feasible to provide system programs and, perhaps more importantly, user source files, "on-line."

To implement this, a disk file system was developed for the 1800. This system provides variable-length, serial-by-character data files to both 1800 and PDP-7 users. Both

symbolic and binary data are kept on-line in this manner. A keyboard utility routine on the 1800 provides simple means to load, dump, list, or copy from or to all 1800 I/O devices and the disk files. Even the approximately tripled listing rate possible with the 1050 printer (15 characters per second, hardware tabs) has been very useful. The pace of program development accelerated greatly as it became possible to be more and more disk-dependent. It was necessary to provide a new text editor because modification of the available one proved impossible. In addition to taking advantage of the device-independent I/O of LOCOSS, the editor provides a couple of string search and replacement commands that are quite useful.

The PDP-7 Assembler was adapted to accept disk file input, although it still punches object code on tape. DDT was made available on-line, and may be loaded and called from LOCOSS. A very powerful macro language, ML-I, was adapted to the disk I/O and made a part of the system. Thus program creation, editing, assembly, debugging, and execution all take place on-line under control of LOCOSS with a minimum of superfluous hard-copy generation.

While the current interface is sufficiently fast for these human-oriented tasks, it will not suffice for the kind of interactive processing desired for the problem-oriented system. Therefore, the authors designed the high-speed general-purpose interface described in this report. It offers flexibility and control substantially beyond current inter-

facing practice as we know it. The general ideas employed in it should be very useful in other multiple computer systems (as opposed to multiple CPU systems with common memory). Implementation of this interface should be completed by the end of 1968; more complete reports on it will be issued later.

PDP-7 System Summary

CPU

8K of 1.75 sec core
18 bits/word
hardware interrupt

Teleprinter (33KSR)

10 chars per second

Paper Tape Reader

8-channel
300 char per second

Paper Tape Punch

8-channel
63 char per second

Dataphone (201A)

synchronous
2000 bits per second
connected to switched network

CRT Display (Modified 338)

A display consisting of a DEC 338, less the PDP-8 portion of the 338, is interfaced to the PDP-7. This is locally known as a 337 and is the prototype for the DEC 339. The display operates asynchronously from instruction files in the PDP-7 memory. It provides point, increment, short vector, vector, and character plotting modes and is capable of branches and subroutining as well as conditional branches, depending on the state of user-controlled switches.

1800 System Summary

CPU(1801C2)

- 16K of 2μsec core
- 16 bits/word + parity and storage protection
- priority interrupt system (12 levels)
- 3 index registers
- 1- and 2-word instruction formats
- 4 data channels

Keyboard-Printer (1816)

- 15 chars/sec

Card Read-Punch (1442)

- read 300 cards per minute
- punch 60 cards per minute

Disk (2310A1)

- 1 drive
- movable head
- interchangeable cartridges (2315)
- 512,000 words per cartridge

II. FUNCTIONAL ORGANIZATION

This report describes the functional design of a high-speed interface between a Digital Equipment Corporation PDP-7 and an IBM 1800. The need for such an interface arose from a desire to integrate both computers into a single system for performing highly interactive, or "conversational," simulations of certain classes of processes.

The PDP-7 is equipped with a cathode-ray-tube display for interactive purposes, and also with a medium-speed (AT&T 201A) dataphone interface for communication with the University's timesharing system. In addition, it has the standard input-output devices: high-speed paper tape reader and punch, and Model 33 KSR teletype. The 1800 is equipped with a one-million-byte disk in addition to the usual I/O devices: card reader and punch, and printer-keyboard.

Effective use of both machines in the simulation system requires that the PDP-7 have access to the 1800's disk, and that the 1800 have access to the PDP-7's display; both of these functions require rapid transfers of data between the two machines.

A relatively low-speed, single-character-at-a-time interface has been in constant use on the above system for the past five months, providing useful experience in the problem of interface design while allowing the development of software for the interactive system to proceed. The new inter-

face will greatly increase the speed of operations currently being performed, and will allow many other functions which are currently impossible or unwieldy.

The principal function of the interface is to transfer blocks of data directly from the core storage of either computer to the core storage of the other. The amount of data to be transferred, and its origin and destination, is specified by registers within the interface. These registers can be loaded by either computer, with or without the active cooperation of the other. Once initialized, the interface transfers data under the control of its own circuitry in conjunction with timing signals generated by the two computers' cycle-steal/data-break facilities; no attention to the transfer is required of either central processing unit. Either computer can, however, detect the status of the interface at any time during a data transfer, and can halt or modify the operation as desired. When a transfer operation has been completed, the interface can interrupt either or both computers, allowing them to process the newly moved data, set up another transmission, or take any other desired action.

Either computer can initiate a data transfer without interfering in any way with the program running in the other machine, and special circuitry has been included to permit reliable resolution of any conficts resulting from simultaneous attempts by both computers to use the interface. Provision is also included for direct interruption of either computer by the other.

The interface performs a parallel-to-serial-to-parallel conversion of the data being transferred, which allows efficient use of the memories of the two computers for storing each other's data since the word size differs for the two machines. This technique also makes it possible to transmit only part of each memory word of the PDP-7 to the 1800, a commonly desired operation.

The interface consists of a Data Register, several control registers, and associated timing and control circuitry. The 34-bit Data Register is composed of a 16-bit (A) and an 18-bit (B) section; the 16-bit section can be loaded in parallel from the 16-bit output bus of the 1800, and the 18-bit section can be loaded in parallel from the 18-bit I/O bus of the PDP-7. Similarly, the 16-bit section of the Data Register can be gated to the input bus of the 1800 while its 18-bit section can be gated to the I/O bus of the PDP-7. The two sections of the Data Register, then, are capable of independent, parallel transfers of data to and from their associated computers, while the Data Register as a whole can be shifted left or right. Serial and parallel operations are performed alternately: data are parallel-transferred from the sending computer to its section of the Data Register, the latter then shifts right or left as necessary to move the data into the other section, and then the data are parallel-transferred from that section to the receiving computer.

2.1 Control Registers

Six control registers are essential to the operation of the interface: these are the A Address Register, the B Address Register, the Unit Count Register, the Status Register, the A Shift Counter, and the B Shift Counter. The first four of these registers are individually addressable. They are capable of being read by either computer, and may also be loaded by either computer (except for certain bits in the Status Register which reflect conditions of the interface not directly controllable by the external machines). The two Address Registers control the address in memory (for their respective computers) to which or from which data will be written or read by the A and B sections of the Data Register. Thus, during an operation in which data are being transferred from the PDP-7 to the 1800, the B Address Register will initially contain the starting address of the block of data in the PDP-7's memory and will be incremented once each time a word is transferred to the interface; similarly for the A Address Register and the 1800. The Unit Count Register initially contains the number of "units" (see later discussion) to transfer and is decremented by one each time a unit transfer is completed. When the Unit Count Register reaches zero, the data transfer operation is considered finished.

The effective word size for each computer is determined by the values loaded into the Shift Counters. The frame size for the 1800 is always 16. For the PDP-7, the frame size is

8, 12, 16, or 18, as specified by a two-bit code in the Status Register. Thus the A Shift Counter is always reloaded with 16 when it counts down to zero, and the B Shift Counter is reloaded as determined by the Status Register frame-size code.

2.2 Data Movement

The following is a detailed description of the events that take place during a transfer from the PDP-7 to the 1800 in the "18/16" mode, and will illustrate the functions of the Data Register and the two Shift counters.

When the "start" command is given, the A Shift Counter is set to 16 and the B Shift Counter to 18. A word is loaded from the PDP-7 into the B portion of the Data Register. Shifting is begun, and both shift count registers are decremented for each bit position shifted. Shifting continues until one of the shift count registers reaches zero. In this case, this will occur after 16 shifts, which have moved the low-order 16 bits of the PDP-7 word into the A portion of the data register. Shifting is suspended until the A part of the data register can be stored in the 1800 memory; then the A Shift Counter is reloaded with 16, and shifting continues. After two more shifts, the B Shift Counter will go to zero. At this point, the two high-order bits of the PDP-7 data word are in the A portion of the data register. Shifting is suspended while the next PDP-7 memory word is loaded into the B portion of the Data Register. Then the B

Shift Counter is reloaded with 18 and shifting resumed. After 14 more shifts, the A Shift Counter will go to zero. The A portion of the Data Register, which now contains two bits of data from one PDP-7 word and 14 bits from the next, will be transferred into the 1800's memory. This process continues in the same manner until both Shift Count Registers go to zero simultaneously. This will occur when an integral number of words has been moved in each machine, and is considered one Unit Operation. The Unit Count Register is then decremented. The entire sequence is started over unless the Unit Count Register has become zero, which signals the end of the transfer operation.

When the user wants to transmit data from the PDP-7 to the 1800 for processing, he uses the "16/16" mode. This mode is very similar to that described above, except that the B Shift Counter is loaded with 16, so that after every right-shift of 16 bits the B section of the Data Register is reloaded with another 18-bit word while the 16-bit A section is being written into the 1800. Reloading the B section after a shift of only 16 places destroys the two high-order bits which remain there; this information is simply lost. However, it is the purpose of this mode to transfer the low-order 16 bits of each word of the PDP-7 to corresponding words in the 1800, preserving the "word" relationships necessary for efficient processing. (Often the data will fit naturally into a 16-bit frame anyway, as when two 8-bit characters are packed

together, so that no useful data at all are lost by transmitting only 16 bits.)

The above two functions, and their inverses, are simply achieved by having the shifting and parallel-transferring of the Data Register controlled by the two Shift Counter registers.

(In more general applications, the frame sizes could be given by two additional loadable and readable Frame Size Registers which could be set as desired at the beginning of each transfer. The A Frame Size Register would be used to load the A Shift Counter each time the latter counts down to zero; similarly for the B Frame Size Register.)

2.3 Control Functions

The control circuits of the interface are able to accept a number of commands, which may be issued by either computer under program control. Most of these commands affect the control registers or other control circuitry; only two of them, Start and Stop, affect the data-handling circuits directly. A Start command causes the interface to begin data transfers as indicated by the control registers, while Stop command halts such an operation at the end of the next unit transfer.

The following is a list of the commands which the interface recognizes, with a short description of each:

a. Start—begins memory-to-memory data transfers as specified by the control registers;

b. Attention—generates an "attention" interruption in the other computer;

c. Test and Seize—examines the Status Register and sets or does not set an indicator bit depending on whether the interface is available or is in use by the other computer (includes provisions for reliable resolution of contention—simultaneous attempts by both computers to seize an available interface);

d. Blast—resets all control circuits and registers, halting immediately any data transmission operation;

e. Sense—makes the contents of the Status Register available for examination to determine the state of the interface;

f. Load—allows any of the control registers to be loaded with data from the computer issuing the command;

g. Store—allows the computer issuing the command to read any of the control registers (into the accumulator of the PDP-7, directly into memory on the 1800);

h. Stop—halts current data transfer at the next unit (integral word) boundary.

The Sense command always brings data into the computer's accumulator, while the Store command specifying the Status Register brings data directly into memory in the case of the 1800.

The Status Register provides detailed control information to both computers and to the interface; the following is a summary thereof:

a. Interface seized by 1800

b. Interface seized by PDP-7

c. Interface busy (data transfer in progress)

d. Operation complete (Unit Count Register = 0)

e. Enable 1800 interruption upon operation-complete

f. Enable PDP-7 interruption upon operation-complete

g. Direction of transmission

h. Exception conditions

i. Attention code

Each of these is indicated by one or more bits in the Status Register.

In order to set up a data transfer, a computer first seizes the interface when it is (becomes) free, then loads the A and B Address Registers with appropriate addresses, loads the Unit Count Register with the length of the data block, and sets the bits of the Status Register to indicate direction of transfer and handling of the operation-complete interruption. It then issues a Start command, and the transfer commences.

Note that the "seized" bits are merely indicators for use by the two computers' software, their main function being the resolution of contention situations; they do not affect either machine's ability to control the interface.

III. INTERACTIVE COMPUTER PROTOCOLS

This interface has simple and unusually flexible control characteristics and allows for a wide range of computer interaction. In cases where one computer has prior knowledge of the desired source or destination of information in the other computer, it can completely initiate the data transfer without interrupting the activity of the other computer. This allows simpler control programs than those where cooperation is required, and requires less time by both machines in servicing the needs of the interface.

The design provides for maximum density of information storage when different sized words are involved in the two computers. The following example will illustrate the flexibility and advantage of the variable frame-size control on each parallel data path.

The PDP-7 has a word consisting of 18 bits. Attached to this computer is a CRT display (modified DEC 338), which uses instructions stored in the memory of the PDP-7. These instructions always occupy the low-order 12 bits of the 18-bit word. Certain other data frequently handled by the PDP-7 consist of only 8 bits per computer word ("character" data) and also 16 bits per computer word ("packed character" data and 1800 instructions). The 1800 has a 16-bit memory word, and also a disk storage device.

The interface described here allows any of the 8-, 12-, 16-, or 18-bit data types to be transferred efficiently to or

from the 1800 and stored by the 1800 on its disk. This interface also allows the 1800 to manipulate the display directly by modifying the display file in PDP-7 core storage without requiring the assistance of the PDP-7.

Since all of the registers of the device can be loaded or read by both machines, they can be used to pass more than one word at a time when the interface is used in a simple "single word" mode.

The following describes a possible computer interaction that can not be achieved with the usual methods:

Suppose that the 1800 is sending a block of data to the PDP-7, and further that the PDP-7 has some information for the 1800 that is of a higher priority than the information currently being transferred. The PDP-7 may opt to stop the current transmission in midstream, load those registers with the control data needed for the desired high-priority transfer, and cause that transfer to take place. When completed, the PDP-7 reloads the interface registers with their contents at the time it was stopped and restarts the previous transfer. Since the completion signals provided by the interface are under the control of the registers, the transfer performed by the PDP-7 need not interrupt the 1800 computer. The 1800 machine will, however, be signaled when its own transfer is completed (if it so desired). Thus the 1800 need not even be aware that the PDP-7-initiated transfer took place except for the change in its memory that resulted. Indeed, the PDP-7 computer could interrupt its own transfer in a similar manner if warranted.

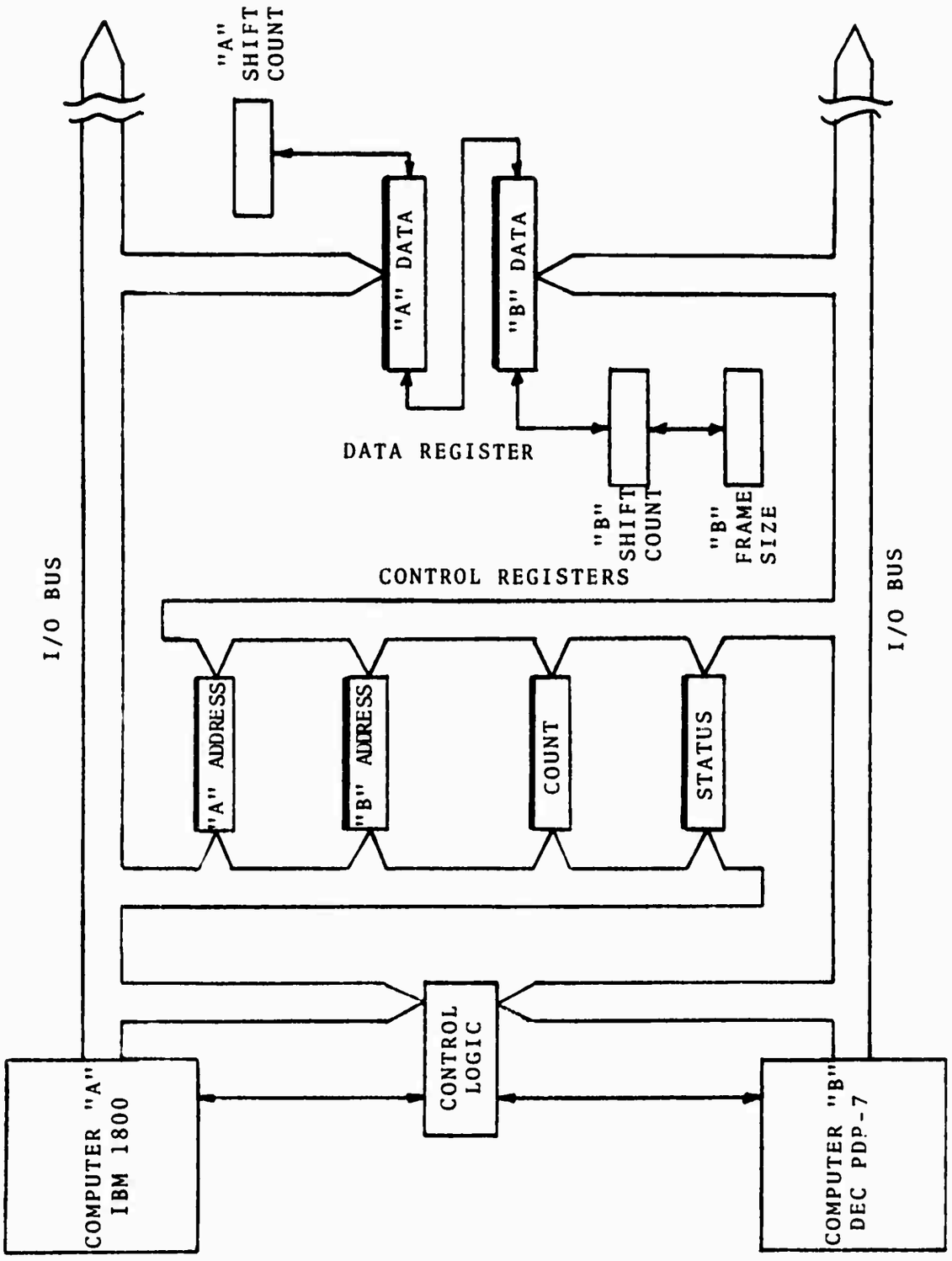

Figure 1. Interface Block Diagram

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DOCUMENT CONTROL DATA - R&D

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1 ORIGINATING ACTIVITY *(Corporate author)*

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2a REPORT SECURITY CLASSIFICATION
Unclassified

2b GROUP

3 REPORT TITLE

FLEXIBLE HIGH-SPEED INTERFACE BETWEEN IBM 1800 and DEC PDP-7 COMPUTERS.

4 DESCRIPTIVE NOTES *(Type of report and inclusive dates)*
Technical Report 12

5 AUTHOR(S) *(Last name, first name, initial)*

R.F. Brender, and J.L. Foy, Jr.

6 REPORT DATE	7a TOTAL NO. OF PAGES	7b NO. OF REFS
November 1968	21	

8a CONTRACT OR GRANT NO.	9a ORIGINATOR'S REPORT NUMBER(S)
DA-49-083 OSA-3050	Technical Report 12
b. PROJECT NO.	
c.	9b OTHER REPORT NO(S) *(Any other numbers that may be assigned this report)*
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14 KEY WORDS	LINK A		LINK B		LINK C	
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IBM 1800						
Interface						
Data Transmission						
Cycle Steal						

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